MOSFET Transistor

DC Analysis

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Outline

1 MOSFET DC Analysis Procedure

2 Examples

3 MOSFET As A Current Source

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Procedure

1. Apply KVL at the gate source loop to find V_{GS}
2. If $V_{GS} < V_{TN}$, the transistor is off. Otherwise, assume an operating region (usually saturation)
3. Use V_{GS} from step 1 to calculate I_D using the transistor current equation
4. Apply KVL at the drain source loop and use I_D from step 3 to find V_{DS}
5. Check the validity of assumed region by comparing V_{DS} to V_{DSAT}
6. Change assumptions and analyze again if required.

- An enhancement-mode device with $V_{DS} = V_{GS}$ is always in saturation
- If we have a source resistance, we need to solve the equations in steps 1 and 3 together to find I_D and V_{GS}.
- If we include channel length modulation or we are in the triode region, we will solve the equations in steps 3 and 4 together
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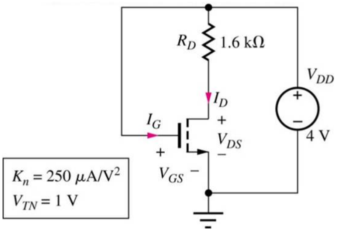

Example

- Find the Q-pt (I_D, V_{DS}) assuming that $V_{TN} = 1V$, and $K_n = 250\mu A/V^2$

Solution

- Assumption: Transistor is saturated, and $I_G = I_B = 0$
- Analysis: From input loop $V_{GS} = V_{DD} = 4V$
- Since the transistor at saturation we can use: $I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2 = \frac{250}{2}\frac{\mu A}{V^2}(4-1)^2 = 1.13mA$

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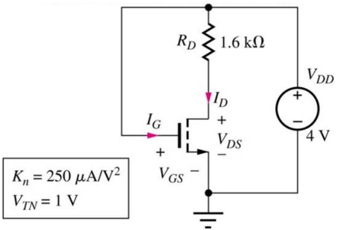

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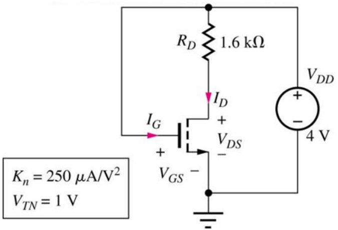

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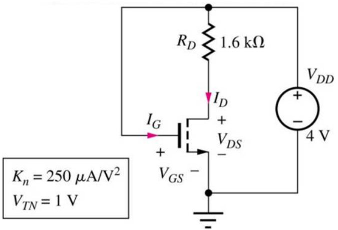

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Example 1

Solution

- Applying KVL at D-S Loop: $V_{DD} = I_D R_D + V_{DS}$
- Substitute by the given values:
  $\therefore 4 = 1.6 * 1.3 + V_{DS} \rightarrow V_{DS} = 2.19V$
- But $V_{DS} < V_{GS} - V_{TN}$. Hence, saturation region assumption is incorrect and the transistor is in triode region.
- Using triode region equation, $4 - V_{DS} = 1600 * 250 \frac{\mu A}{V^2} (4 - 1 - \frac{V_{DS}}{2}) V_{DS}$
- Solving the last equation $\therefore V_{DS} = 2.3V$, and $I_D = 1.06mA$
- $V_{DS} < V_{GS} - V_{TN}$, transistor is in triode region
- Q-pt: (1.06 m.A, 2.3 V) with V_{GS}= 4 V

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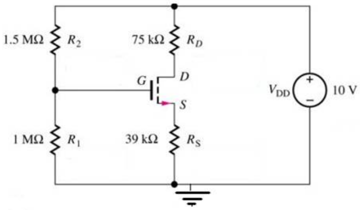

Example

- Find the Q-pt (I_D, V_{DS}) assuming that V_{TN}=1V, and $K_n = 25\mu A/V^2$

Solution

- Approach: Assume operation region, find Q-point, check to see if result is consistent with operation region
- Assumption: Transistor is saturated, $I_G = I_B = 0$
- Analysis: First, simplify circuit, split V_{DD} into two equal-valued sources and apply Thevenin's transformation to find V_{EQ} and R_{EQ} for the gate-bias voltage

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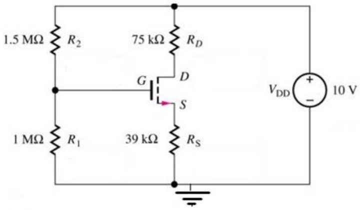

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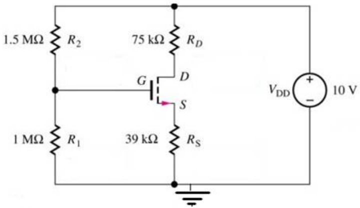

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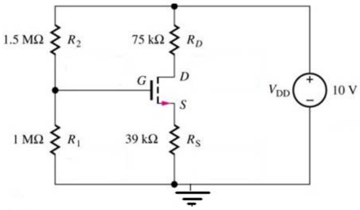

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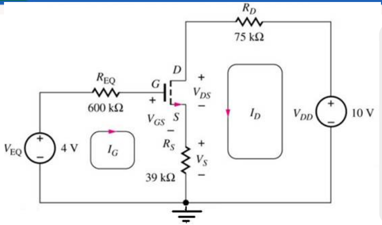

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- Substitute by given values $4 = V_{GS} + \frac{(25\times10^{-6})(39\times10^{3})}{2}(V_{GS}-1)^2$
- Solving the quadratic equation results in $V_{GS} = -2.71V, +2.66V$
- Since $V_{GS} < V_{TN}$ for V_{GS} = -2.71 V, we will ignore it
- Substituting with V_{GS} = +2.66 V results in $I_D = 34.4\mu A$
- Applying KVL at D-S loop, $V_{DD} = I_D(R_D + R_S) + V_{DS} \rightarrow V_{DS} = 6.08V$
- Since $V_{DS} > V_{GS} - V_{TN}$. Hence saturation region assumption is correct.
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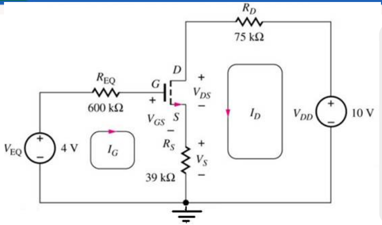

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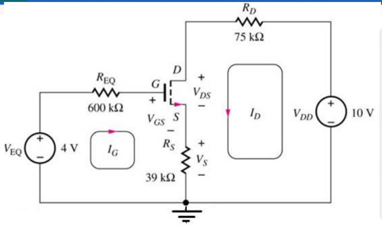

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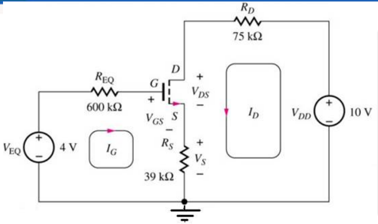
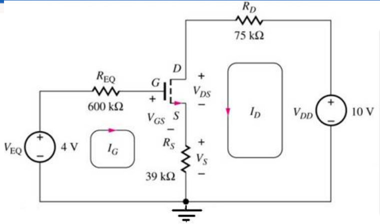


- Apply KVL at G-S Loop: $V_{EQ} = V_{GS} + I_D R_S$
- Using $I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2$
- $\therefore V_{EQ} = V_{GS} + \frac{K_n R_S}{2}(V_{GS} - V_{TN})^2$

- Substitute by given values $4 = V_{GS} + \frac{(25\times10^{-6})(39\times10^{3})}{2}(V_{GS} - 1)^2$
- Solving the quadratic equation results in $V_{GS} = -2.71V, +2.66V$
- Since $V_{GS} < V_{TN}$ for V_{GS} = -2.71 V, we will ignore it
- Substituting with V_{GS} = +2.66 V results in $I_D = 34.4\mu A$
- Applying KVL at D-S loop, $V_{DD} = I_D(R_D + R_S) + V_{DS} \rightarrow V_{DS} = 6.08V$
- Since $V_{DS} > V_{GS} - V_{TN}$. Hence saturation region assumption is correct.
- Q-pt: (34.4 μA, 6.08 V) with V_{GS}= 2.66 V

Example 2
Solution



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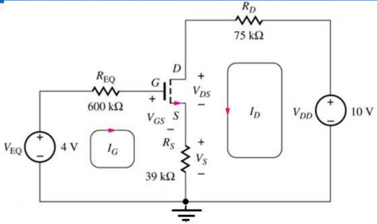

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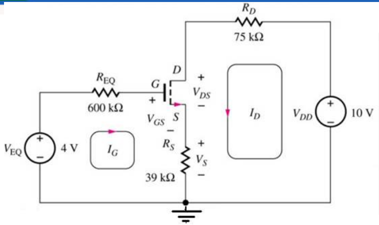

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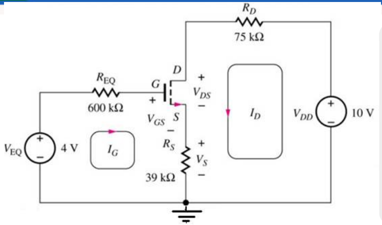

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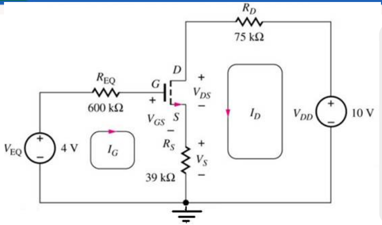

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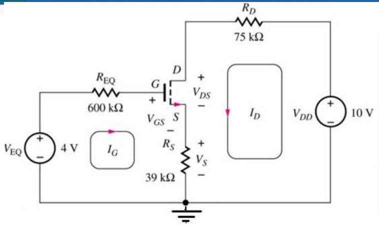

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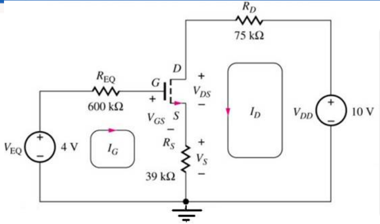

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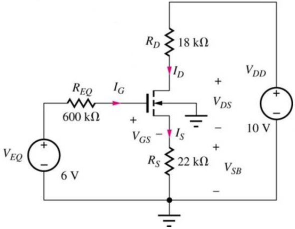
Example 3

Bias Analysis with Body Effect



Example

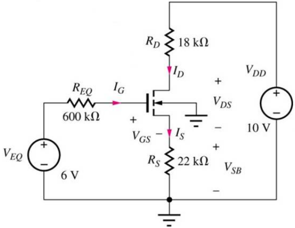
- Find the Q-pt (I_D, V_{DS}) assuming that $V_{TO} = 1V, 2\phi_F = 0.6V, \gamma = 0.5\sqrt{V}$, and $K_n = 25\mu A/V^2$

Solution

- Approach: Assume operation region, find Q-point, check to see if result is consistent with operation region
- Assumption: Transistor is saturated, $I_G = I_B = 0$
- Analysis: First, using KVL at the G-S loop yields: $V_{GS} = V_{EQ} - I_D R_S = 6 - 22,000 I_D$

Example 3

Bias Analysis with Body Effect



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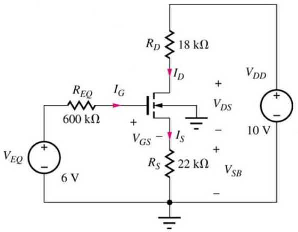

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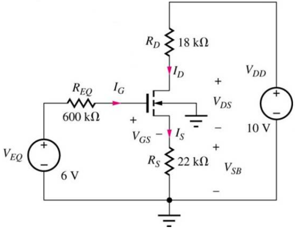

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Solution

- Since $V_{SB} \neq 0$ then use $V_{TN} = V_{TO} + \gamma(\sqrt{V_{SB} + 2\varphi_F} - \sqrt{2\varphi_F})$
- $\therefore V_{TN} = 1 + 0.5(\sqrt{22000 I_D + 0.6} - \sqrt{0.6})$
- Using $I'_D = \frac{(25 \times 10^{-6})}{2}(V_{GS} - V_{TN})^2$ we can solve the non-linear equation to find I_D or use the iteration method below

Iteration Method

- Estimate value of I_D and use it to find V_{GS} and V_{TN}
- Find I'_D using V_{GS} and V_{TN} from the last step
- If I'_D is not same as original I_D estimate, start again.

- The iteration sequence leads to I_D= 88.0 μA
- Applying KVL at D-S loop,
  $V_{DS} = V_{DD} - I_D(R_D + R_S) = 10 - 40,000 I_D = 6.48 V$
- Since $V_{DS} > V_{GS} - V_{TN}$. Hence saturation region assumption is correct.
- Q-pt: (88 μA, 6.48 V) with V_{GS}= 4.06 V

Example 3

Solution

- Since $V_{SB} \neq 0$ then use $V_{TN} = V_{TO} + \gamma(\sqrt{V_{SB} + 2\varphi_F} - \sqrt{2\varphi_F})$
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Solution

- Since $V_{SB} \neq 0$ then use $V_{TN} = V_{TO} + \gamma(\sqrt{V_{SB} + 2\varphi_F} - \sqrt{2\varphi_F})$
- $\therefore V_{TN} = 1 + 0.5(\sqrt{22000 I_D + 0.6} - \sqrt{0.6})$
- Using $I_D' = \frac{(25\times10^{-6})}{2}(V_{GS} - V_{TN})^2$ we can solve the non-linear equation to find I_D or use the iteration method below

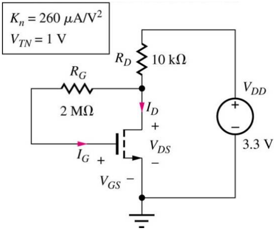
Iteration Method

- Estimate value of I_D and use it to find V_{GS} and V_{TN}
- Find I_D' using V_{GS} and V_{TN} from the last step
- If I_D' is not same as original I_D estimate, start again.

- The iteration sequence leads to I_D= 88.0 μA
- Applying KVL at D-S loop,
  $V_{DS} = V_{DD} - I_D(R_D + R_S) = 10 - 40,000 I_D = 6.48 V$
- Since $V_{DS} > V_{GS} - V_{TN}$. Hence saturation region assumption is correct.
- Q-pt: (88 μA, 6.48 V) with V_{GS}= 4.06 V

Example 4

Bias with Feedback



Example

- Find the Q-pt (I_D, V_{DS}) assuming that $V_{TN} = 1V$, and $K_n = 260\mu A/V^2$

Solution

- Assumption: $I_G = I_B = 0$
- Analysis: Transistor is saturated since $V_{DS} = V_{GS}$
- Using KVL at the D-S loop yields: $V_{DS} = V_{GS} = V_{DD} - I_D R_D$

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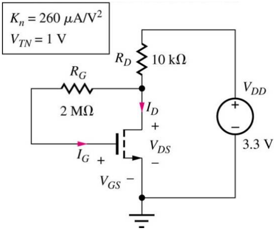

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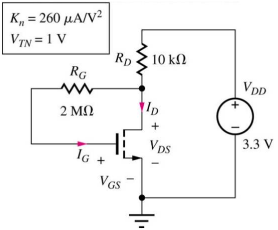

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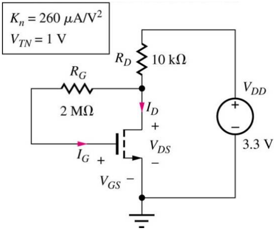

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Example 4

Solution

- Since the transistor at saturation we can use: $I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2$
- Substitute in the last KVL equation yields:
  $V_{GS} = V_{DD} - \frac{K_n R_D}{2}(V_{GS} - V_{TN})^2$
- Substitute by the given values:
  $\therefore V_{GS} = 3.3 - \frac{(2.6\times10^{-4})(10^4)}{2}(V_{GS} - 1)^2$
- Solve the quadratic equation : $\therefore V_{GS} = -0.769V, +2.00V$
- Since $V_{GS} < V_{TN}$ for V_{GS}= -0.769 V and MOSFET will be cut-off, it will be ignored.
- Substitute in the current equation yields: $I_D = 130\mu A$
- Q-pt: (130 μA, 2 V) with V_{GS}= 2 V

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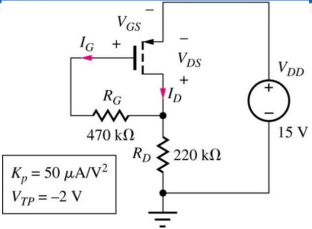
Example 5

Enhancement PMOS



Example

- Find the Q-pt (I_D, V_{DS}) assuming that $V_{TP} = -2V$, and $K_p = 50\mu A/V^2$

Solution

- Assumption: $I_G = I_B = 0$
- Analysis: Transistor is saturated since $V_{SD} = V_{SG}$
- Applying KVL at D-S loop: $-15V + (220k\Omega)I_D + V_{SG} = 0$
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- $\therefore V_{SG} = 0.369V, 3.45V$
- Since $V_{SG} = 0.369V < |V_{TP}| = 2$ V, $\therefore V_{SG} = 3.45$ V and $I_D = 52.5$ mA.
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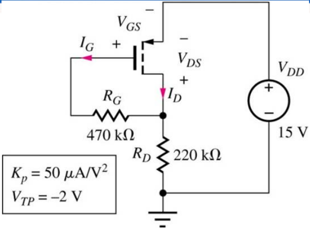
Example 5

Enhancement PMOS



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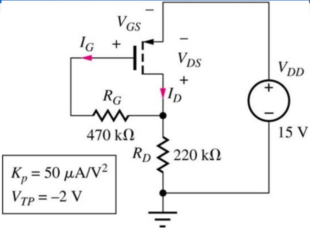

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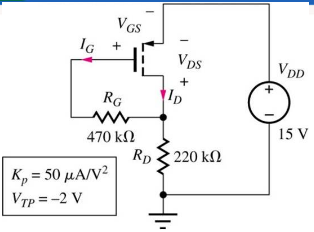

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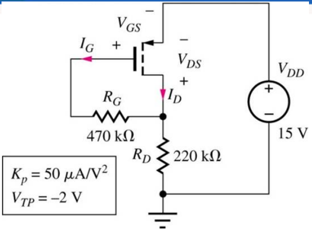

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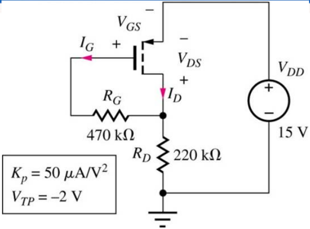

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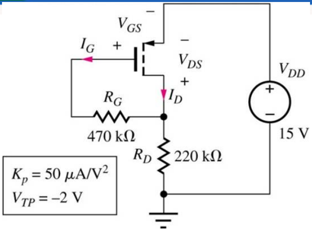

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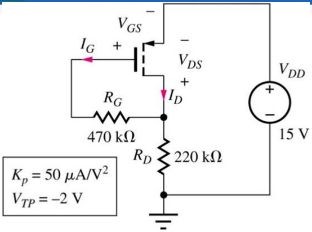

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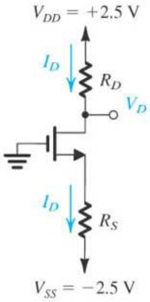


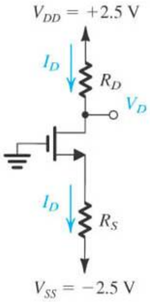
Example

Design the shown circuit so that the transistor operates at $I_D = 0.3m.A$ and $V_D = +0.4V$. The NMOS transistor has $V_t = 1V, \mu_n C_{ox} = 60\mu A/V^2, L = 3\mu m,$ and $W = 120\mu m$.

Answer

- $R_S = 3.3k\Omega$, and $R_D = 7k\Omega$

Example 6



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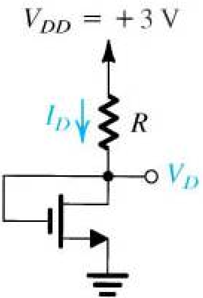

Example

Design the shown circuit so that the transistor operates at $I_D = 80\mu A$. The NMOS transistor has $V_t = 0.6V$, $\mu_n C_{ox} = 200\mu A/V^2$, $L = 0.8\mu m$, and $W = 4\mu m$. Also, find the drain voltage V_D.

Answer

- $R = 25k\Omega$, and $V_D = +1V$

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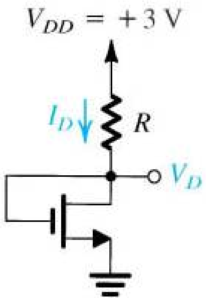

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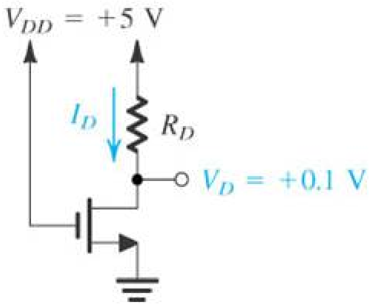


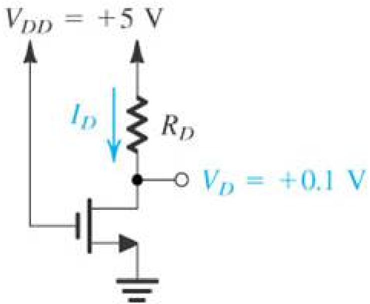
Example

Design the shown circuit to establish V_D of 0.1 V. The NMOS transistor has $V_t = 1V$, and $k_n' W/L = 1mA/V^2$. What is the effective resistance between drain and source at this operating point?.

Answer

- $R_D = 12.4k\Omega$, and $r_{ds} = 253\Omega$

Example 8



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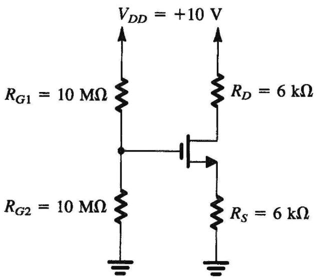


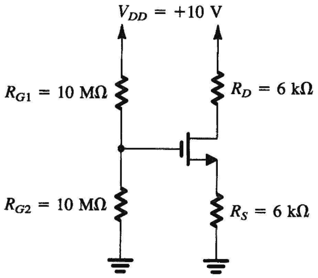
Example

Analyze the circuit shown to determine the voltages at all nodes and the currents through all branches. The NMOS transistor has $V_t = 1V$, and $k_n' W/L = 1mA/V^2$.

Answer

- $I_G = 0mA$, $I_{RG} = 0.5\mu A$, $I_D = 0.5mA$, $V_G = 5V$, $V_S = +3V$, and $V_D = +7V$

Example 9



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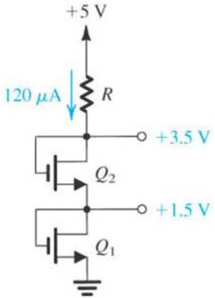
Example 10



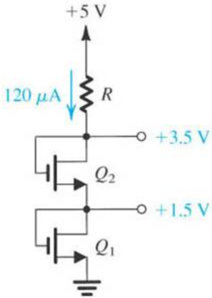
Example

Design the shown circuit to obtain the indicated current and voltage values. The NMOS transistor has $V_t = 1V, \mu_n C_{ox} = 120\mu A/V^2, \lambda = 0,$ and $L_1 = L_2 = 1\mu m$.

Answer

- $R = 12.5k\Omega, W_1 = 8\mu m,$ and $W_1 = 2\mu m$

Example 10



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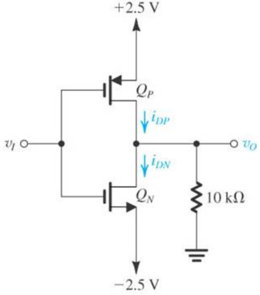
Answer

- $R = 12.5k\Omega$, $W_1 = 8\mu m$, and $W_1 = 2\mu m$

Example 11



Example

For the shown circuit calculate the shown current and voltage values for v_I = 0V, +2.5V, and -2.5V. Assuming matched transistors with $V_{TN} = V_{TP} = 1V, k_n = k_p = 1mA/V^2$, and $\lambda = 0$.

Answer

- $I_{DN} = I_{DP} = 1.125mA$, and $v_o = 0V$
- $I_{DN} = 0.244mA$, $I_{DP} = 0mA$, and $v_o = -2.44V$
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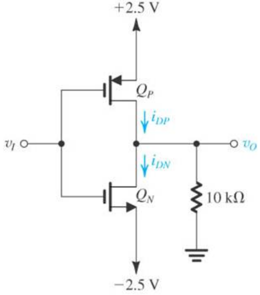

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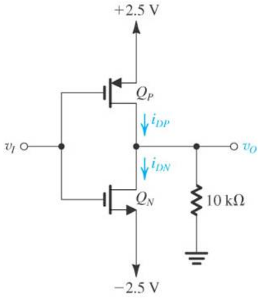

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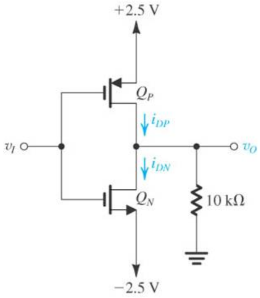

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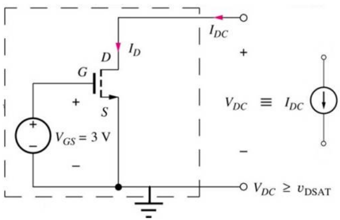
Outline

1 MOSFET DC Analysis Procedure

2 Examples

3 MOSFET As A Current Source

MOSFET As A Current Source

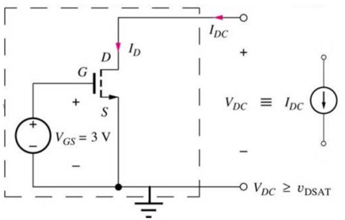


- Ideal current source gives fixed output current regardless of the voltage across it.
- MOSFET behaves as as an ideal current source if biased in the pinch-off region (output current depends on terminal voltage).

Notes

- V_{DS} should be greater than V_{DSAT} for proper operation
- If the channel length modulation isn't neglected, a finite source resistance will exist $= [\lambda I_D]^{-1}$

MOSFET As A Current Source



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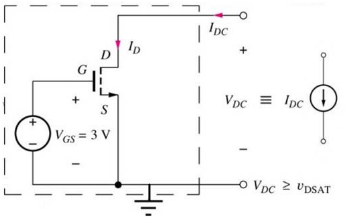

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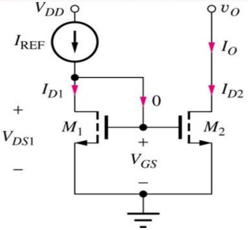
MOSFET As A Current Source

Current Mirror



- Assumptions: M_1 and M_2 have identical V_{TN}, K_n', λ and are in saturation.

Analysis

- $I_{REF} = \frac{K_n'}{2}\left(\frac{W}{L}\right)_{M1}(V_{GS1} - V_{TN})^2(1 + \lambda V_{DS1})$
- $I_O = \frac{K_n'}{2}\left(\frac{W}{L}\right)_{M2}(V_{GS2} - V_{TN})^2(1 + \lambda V_{DS2})$
- But $V_{GS2} = V_{GS1}$, $\therefore I_O = I_{REF}\frac{\left(\frac{W}{L}\right)_{M2}}{\left(\frac{W}{L}\right)_{M1}}\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})} \simeq \frac{\left(\frac{W}{L}\right)_{M2}}{\left(\frac{W}{L}\right)_{M1}} I_{REF}$
- Thus, output current mirrors reference current if $V_{DS1} = V_{DS2}$ or $\lambda = 0$, and both transistors have the same (W/L).

MOSFET As A Current Source

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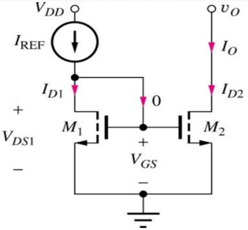

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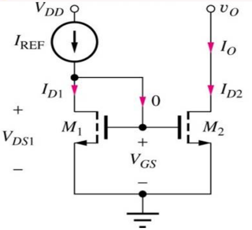

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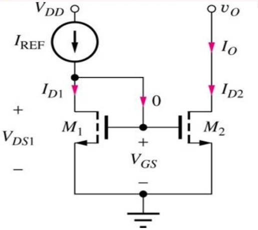

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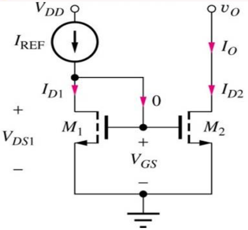

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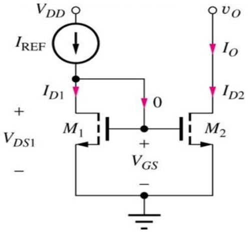
Current Mirror



Example

Find the output current and the minimum output voltage v_o to maintain the given current mirror in proper operation. Assume, I_{REF}= 50 μ A, V_O= 12 V, V_{TN} = 1 V, K_n'= 75 $\mu A/V^2$, $\lambda = 0V^{-1}$, $(W/L)_{M1} = 2$, $(W/L)_{M2}$=10

Analysis

- $\therefore I_O = I_{REF}\frac{\left(\frac{W}{L}\right)_{M2}}{\left(\frac{W}{L}\right)_{M1}} = 250\mu A$
- $V_{GS} = V_{TN} + \sqrt{\frac{2I_{REF}}{K_n'\left(\frac{W}{L}\right)(1+\lambda V_{DS1})}} = 1V + \sqrt{\frac{2(50\mu A)}{2*75\frac{\mu A}{V^2}}} = 1.82V$
- Hence, $V_{omin} = V_{GS} - V_{TN} = 0.82V$.

Example 12

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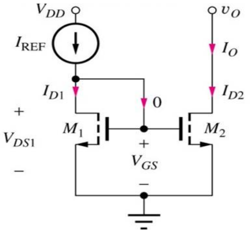

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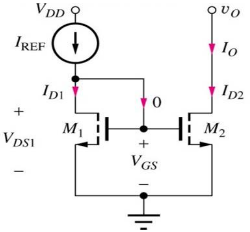

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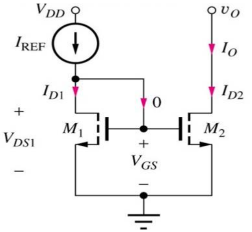

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